CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of obtaining a signal from a pixel cell comprising:

generating charges with a photodetector during an integration period;

resetting a charge storage node that receives charges generated by said photodetector to a reset level;

with the storage node at the reset level, reading and sampling a first output signal from a capacitive transimpedance amplifier having an input coupled to said storage node;

receiving charges at said charge storage node generated by said photodetector; and

reading and sampling a second output signal from said capacitive transimpedance amplifier after said integration period.

2. The method of claim 1 further comprising obtaining a difference signal indicating a difference between said first and second output signals.

3. The method of claim 1 in which resetting said storage node and reading and sampling the first output signal are performed before reading and sampling the second output signal.

4. The method of claim 1 further comprising operating said capacitive transimpedance amplifier in an open loop during said integration period.

5. The method of claim 1, wherein said resetting resets a capacitor of said capacitive transimpedance amplifier.

6. The method of claim 1, wherein said charge storage node is part of said photodetector.

7. The method of claim 1, wherein said charge storage node is a floating diffusion node which receives charges from said photodetector and said resetting resets said floating diffusion node.

8. The method of claim 1 further comprising providing a lower power to the capacitive transimpedance amplifier during said integration period and a higher power during said reading and sampling operations.

9. The method of claim 1 further comprising providing no power to the capacitive transimpedance amplifier during said integration period.

10. The method of claim 1 further comprising controlling a charge transference from the photodetector to said storage node with a transfer gate transistor.

11. The method of claim 1 further comprising operating at least a portion of said capacitive transimpedance amplifier outside of a pixel cell.

12. The method of claim 1 further comprising operating a portion of said capacitive transimpedance amplifier outside of a pixel cell and a portion of said capacitive transimpedance amplifier inside a pixel cell.

13. The method of claim 1 further comprising operating a capacitive transimpedance amplifier inside a pixel cell.

14. A method of operating a pixel cell, the method comprising:

generating photogenerated charges with a photodetector during an integration period;

operating a capacitive transimpedance amplifier at a first lower power level during said integration period; and

amplifying said charges generated by said photodetector with said capacitive transimpedance amplifier operating at a second higher power level during a readout period.

15. The method of claim 14, wherein said first power level equals zero watts.

16. The method of claim 14 further comprising biasing the photodetector to a sufficient voltage before the integration period to maintain the photodetector in a reverse bias condition during said integration period.

17. The method of claim 14 further comprising operating said capacitive transimpedance amplifier in an open loop during said integration period.

18. A method of operating a pixel cell, the method comprising:

integrating a charge signal by a photodetector during an integration period; and

operating a capacitive transimpedance amplifier which receives charges from said photodetector in an open loop condition during said integration period.

19. The method of claim 18 further comprising discharging a storage node which receives charges generated by said photodetector from a first state to a second state during the integration period.

20. The method of claim 18 further comprising operating a portion of said capacitive transimpedance amplifier outside of said pixel cell.

21. The method of claim 20, wherein said operating occurs during a readout period.

22. The method of claim 18 further comprising resetting said photodetector and a capacitor of said capacitive transimpedance amplifier with a reset switch.

23. The method of claim 19 further comprising controlling a charge transference from the photodetector to said storage node with a transfer transistor.

24. A method of operating a pixel cell, the method comprising:

providing first and second bias voltages to operate a capacitive transimpedance amplifier;

generating charges with a photodetector during an integration period;

resetting a charge storage node that receives photo generated charges generated by said photodetector to a reset level;

with the storage node at the reset level, reading and sampling a first output signal from said capacitive transimpedance amplifier having an input coupled to said storage node;

closing a switch circuit to float a reset line to operate said capacitive transimpedance amplifier during a readout operation;

receiving charges at said charge storage node generated by said photodetector during said integration period; and

reading and sampling a second output signal from said capacitive transimpedance amplifier after said integration period.

25. The method of claim 24 further comprising controlling said switch circuit by pulsing a row select line.

26. The method of claim 24 further comprising operating at least a portion of said capacitive transimpedance amplifier outside of said pixel cell.

27. The method of claim 24 further comprising operating a portion of said capacitive transimpedance amplifier outside of said pixel cell and operating a portion of said capacitive transimpedance amplifier inside said pixel cell.

28. The method of claim 24 further comprising operating said capacitive transimpedance amplifier within said pixel cell.

29. The method of claim 24 further comprising controlling a charge transference from the photodetector to said storage node with a transfer transistor.

30. A pixel circuit comprising:

a photodetector that generates charge;

a storage node for receiving charge generated by said photodetector;

an amplifier having an input coupled to said storage node and an output that provides an amplified input signal;

a feedback capacitor, said capacitor providing feedback between the amplifier's output and input; and

a reset switch that resets said storage node when closed.

31. The circuit of claim 30 further comprising a transfer transistor that transfers said charge from said photodetector to said storage node and a switch for selectively connecting one of a first and second power source to said amplifier.

32. The circuit of claim 31, wherein an output power of said second power source is greater than an output power of said first power source.

33. The circuit of claim 30, wherein said storage node is part of said photodetector.

34. The circuit of claim 30, wherein said storage node is a floating diffusion node separate from said photodetector.

35. The circuit of claim 30, wherein said reset switch resets said feedback capacitor when closed.

36. The circuit of claim 33, wherein said reset switch resets said photodetector from a reset voltage line when closed.

37. The circuit of claim 30 further comprising a select switch, said select switch connecting the amplifier output to a column line when closed.

38. The circuit of claim 30, wherein an output stage of said amplifier resides outside of a pixel array.

39. The circuit of claim 30, wherein said amplifier is configured as a folded four-transistor cascode amplifier.

40. The circuit of claim 34 further comprising a transfer transistor that transfers said charge from said photodetector to said amplifier.

41. The circuit of claim 39 further comprising a switch circuit that connects a pixel to a column line.

42. The circuit of claim 30 further comprising a reset transistor that resets said photodetector and said feedback capacitor.

43. An integrated circuit comprising:

a pixel array with rows and columns of pixel cells, and, for each column, a column readout line that connects to the column's pixel cells; each pixel cell including:

a photodetector that provides a first signal indicating detected light;

an amplifier with an input that receives the first signal and an output that provides an output signal based on the first signal; and

feedback capacitance that provides feedback from the amplifier output to the amplifier input; and

readout circuitry connected to the column readout line, the readout circuitry providing readout signals from the column pixel cells; the readout circuitry including sampling circuitry for sampling the amplifier output signal.

44. The integrated circuit of claim 43 in which each pixel cell further comprises a transfer transistor that transfers said charge from said photodetector to said amplifier.

45. The integrated circuit of claim 43, wherein said amplifier selectively receives a reset signal and a charge generated signal at an input, said sampling circuitry obtaining a reset sample and a charge signal sample from said amplifier output.

46. The integrated circuit of claim 43, in which the amplifier and feedback capacitor form a capacitive transimpedance amplifier.

47. The integrated circuit of claim 43 in which the amplifier includes an input transistor and an output stage.

48. The integrated circuit of claim 43 in which the amplifier is a single ended four-transistor cascode amplifier.

49. The integrated circuit of claim 48 further comprising a transfer transistor that transfers said charge from said photodetector to said amplifier.

50. The integrated circuit of claim 43, wherein the readout circuitry further includes amplifier output stage circuitry; when each pixel cell is connectable to a column line, the amplifier and the output stage circuitry forming a distributed amplifier.

51. The integrated circuit of claim 43 in which each pixel cell further comprises a switch for selectively connecting one of a first and second power source to said amplifier.

52. An integrated circuit comprising:

a pixel array with rows and columns of pixel cells and, for each column, a column readout line that connects to pixel cells of a column; each pixel cell including:

a photodetector that provides a first signal indicating detected light;

an amplifier with an input that receives the first signal and an output that provides signals based on the first signal; and

feedback capacitance that provides feedback from the amplifier output to the amplifier input; and

readout circuitry connected to the column readout line, the readout circuitry providing readout signals from a column line; the readout circuitry including:

amplifier output stage circuitry arranged such that when the pixel cell is connected to a column line the amplifier and the output stage circuitry form a distributed amplifier.

53. The integrated circuit of claim 52 in which the output stage circuitry is outside the pixel array.

54. The integrated circuit of claim 52 in which the pixel array further includes select circuitry that connects a pixel cell to an associated column readout line in response to a row select signal.

55. The integrated circuit of claim 52, wherein said distributed amplifier is configured as a single ended four-transistor cascode amplifier.

56. The integrated circuit of claim 52, wherein said distributed amplifier is configured as a folded four-transistor cascode amplifier.

57. The integrated circuit of claim 52 wherein said distributed amplifier is configured as a differential input telescopic cascode amplifier.

58. The integrated circuit of claim 52 further comprising a transfer transistor that transfers said charge from said photodetector to said amplifier.

59. The integrated circuit of claim 58, wherein said distributed amplifier is configured as a single ended four-transistor cascode amplifier.

60. The integrated circuit of claim 58, wherein said distributed amplifier is configured as a folded four-transistor cascode amplifier.

61. The integrated circuit of claim 58 wherein said distributed amplifier is configured as a differential input telescopic cascode amplifier.

62. The integrated circuit of claim 52, wherein said photodetector senses visible light.

63. The integrated circuit of claim 52, wherein said photodetector senses infrared light.

64. The integrated circuit of claim 52 in which each pixel cell further includes a reset switch that, when closed, resets the photodetector to a reset level.

65. The integrated circuit of claim 52 in which each pixel further includes a reset switch that, when closed, resets the photodetector and the amplifier to a reset level.

66. The integrated circuit of claim 52 in which each pixel further includes a reset switch that, when closed, resets the amplifier and a floating diffusion node coupled to the photodetector and to the input of said amplifier.

67. The integrated circuit of claim 52 in which the readout circuitry further includes a sampling circuit connected to said column readout line.

68. An imaging circuit comprising:

an array of pixels, each pixel including:

a photodetector that generates charge in response to light;

a storage node for storing charges generated by said photodetector;

an amplifier that amplifies a signal received from said storage node;

a feedback capacitor that provides feedback to an input of the amplifier; and

a reset switch that resets a storage node when closed; and

69. The circuit of claim 68, wherein said amplifier is a capacitive transimpedance amplifier.

70. The circuit of claim 68, wherein at least a portion of said amplifier is located outside said array of pixels.

71. The circuit of claim 68 in which the array further comprises, for each pixel cell, a first select switch that connects said capacitor and said reset switch to the amplifier output circuit when closed.

72. The circuit of claim 68 in which the array further comprises, for each pixel cell, a second select switch that connects the amplifier input to the amplifier output circuit when closed.

73. The circuit of claim 68 in which the array further comprises, for each pixel, a transfer transistor that transfers charge from said photodetector to said amplifier.

74. The circuit of claim 68, wherein said amplifier is a distributed amplifier configured as a folded four-transistor cascode amplifier.

75. A pixel sensor array comprising:

an array of pixel cells, each pixel cell including:

a photodetector that generates charge in response to light;

an amplifier that amplifies a signal received from said photodetector;

a feedback capacitor that provides feedback to the input of the amplifier; and

a reset switch that resets the photodetector from a reset voltage line when closed.

76. The array of claim 75 in which each pixel cell further comprises a transfer transistor that transfers charge from said photodetector to said amplifier.

77. An imaging system comprising:

a processor;

an imaging device coupled to said processor, the imaging device comprising:

an array of pixels, each pixel including:

a photodetector that generates charge in response to light;

a storage node for storing charges generated by said photodetector;

an amplifier that amplifies charges on said storage node;

a feedback capacitor that provides feedback to an input of the amplifier; and

a reset switch that resets the storage node when closed; and

amplifier output circuitry located outside the pixel array; the amplifier, the amplifier output circuitry, and the feedback capacitor together forming a capacitive transimpedance amplifier.

78. The system of claim 77 in which each pixel further comprises a first transfer transistor that transfers charge from said photodetector to said storage node.

79. The system of claim 77 in which the imaging device further comprises a sampling circuit that samples the output of said amplifier.

80. The system of claim 77, wherein said capacitive transimpedance amplifier is configured as a single ended four-transistor cascode amplifier.

81. The system of claim 77, wherein said capacitive transimpedance amplifier is configured as a folded four-transistor cascode amplifier.

82. The system of claim 77, wherein said capacitive transimpedance amplifier is configured as a differential input telescopic cascode amplifier.

83. The system of claim 77, wherein said storage node is part of said photodetector and said reset switch resets said photodetector when closed.

84. The system of claim 77, wherein said storage node is a floating diffusion node separate from said photodetector and said reset switch resets said floating diffusion node when closed.